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<p>(21) International Application Number: PCT/US99/06306 (22) International Filing Date: 22 March 1999 (22.03.99) (30) Priority Data: 09/045,245 20 March 1998 (20.03.98) US 60/085,675 15 May 1998 (15.05.98) US (71) Applicant (for all designated States except US): SEMITOOL, INC. [US/US]; 655 Reserve Drive, Kalispell, MT 59901 (US). (72) Inventor; and (75) Inventor/Applicant (for US only): CHEN, Linlin [CA/US]; 121 Hawthorne Avenue, Kalispell, MT 59901 (US). (74) Agent: ERICKSON, Randall, T.; Rockey, Milnamow & Katz, Ltd., Two Prudential Plaza, 47th floor, 180 North Stetson, Chicago, IL 60601 (US).</p>		<p>(81) Designated States: CN, JP, KR, SG, US, European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE). Published With international search report.</p>
<p>(54) Title: APPARATUS AND METHOD FOR ELECTROLYTICALLY DEPOSITING COPPER ON A SEMICONDUCTOR WORK- PIECE</p>		
<p>(57) Abstract</p> <p>This invention employs a novel approach to the copper metallization of a workpiece, such as a semiconductor workpiece. In accordance with the invention, an alkaline electrolytic copper bath (35) is used to electroplate copper onto a seed layer (30), electroplate copper directly onto a barrier layer material, or enhance an ultra-thin copper seed layer which has been deposited on the barrier layer using a deposition process such as PVD. The resulting copper layer provides an excellent conformal copper coating that fills trenches, vias, and other microstructures in the workpiece. When used for seed layer enhancement, the resulting copper seed layer provides an excellent conformal copper coating that allows the microstructures to be filled with a copper layer having good uniformity using electrochemical deposition techniques. Further, copper layers that are electroplated in the disclosed manner exhibit low sheet resistance and are readily annealed at low temperatures.</p>		

- 1 -

TITLE OF THE INVENTION

APPARATUS AND METHOD FOR ELECTROLYTICALLY DEPOSITING
COPPER ON A SEMICONDUCTOR WORKPIECE

BACKGROUND OF THE INVENTION

In the fabrication of microelectronic devices, application of one or more metallization layers is often an important step in the overall fabrication process. The metallization may be used in the formation of discrete microelectronic components, such as read/write heads, but it is more often used to interconnect components formed on a workpiece, such as a semiconductor workpiece. For example, such structures are used to interconnect the devices of an integrated circuit.

A basic understanding of certain terms used herein will assist the reader in understanding the disclosed subject matter. To this end, basic definitions of certain terms, as used in the present disclosure, are set forth below.

Single Metallization Level is defined as a composite level of a

- 3 -

limit the performance of integrated circuits. More particularly, these delays limit the speed at which an integrated circuit may process these electrical signals. Larger propagation delays reduce the speed at which the integrated circuit may process the electrical signals, while smaller propagation delays increase this speed. Accordingly, integrated circuit manufacturers seek ways in which to reduce the propagation delays.

For each interconnect path, signal propagation delay may be characterized by a time delay τ . See E.H. Stevens, *Interconnect Technology*, QMC, Inc., July 1993. An approximate expression for the time delay, τ , as it relates to the transmission of a signal between transistors on an integrated circuit is given below.

$$\tau = RC[1 + (V_{SAT}/RI_{SAT})]$$

In this equation, R and C are, respectively, an equivalent resistance and capacitance for the interconnect path and I_{SAT} and V_{SAT} are, respectively, the saturation (maximum) current and the drain-to-source potential at the onset of current saturation for the transistor that applies a signal to the interconnect path. The path resistance is proportional to the resistivity, ρ , of the conductor material. The path capacitance is proportional to the relative dielectric permittivity, K_e , of the dielectric material. A small value of τ requires that the interconnect line carry a

- 5 -

workpieces have been developed in recent years. One such process is chemical vapor deposition (CVD), in which a thin copper film is formed on the surface of the barrier layer by thermal decomposition and/or reaction of gas phase copper compositions. A CVD process can result in conformal copper coverage over a variety of topological profiles, but such processes are expensive when used to implement an entire metallization layer.

Another known technique, physical vapor deposition (PVD), can readily deposit copper on the barrier layer with relatively good adhesion when compared to CVD processes. One disadvantage of PVD processes, however, is that they result in poor (non-conformal) step coverage when used to fill microstructures, such as vias and trenches, disposed in the surface of the semiconductor workpiece. For example, such non-conformal coverage results in less copper deposition at the bottom and especially on the sidewalls of trenches in the semiconductor devices.

Inadequate deposition of a PVD copper layer into a trench to form an interconnect line in the plane of a metallization layer is illustrated in Fig. 1. As illustrated, the upper portion of the trench is effectively "pinched off" before an adequate amount of copper has been deposited within the lower portions of the trench. This results in an open void region that seriously impacts the ability of the metallization line to carry the electrical signals for which it was designed.

Electrochemical deposition of copper has been found to provide the most

- 7 -

BRIEF SUMMARY OF THE INVENTION

This invention employs a novel approach to the copper metallization of a workpiece, such as a semiconductor workpiece. In accordance with the invention, an alkaline electrolytic copper bath is used to electroplate copper onto a seed layer, electroplate copper directly onto a barrier layer material, or enhance an ultra-thin copper seed layer which has been deposited on the barrier layer using a deposition process such as PVD. The resulting copper layer provides an excellent conformal copper coating that fills trenches, vias, and other microstructures in the workpiece. When used for seed layer enhancement, the resulting copper seed layer provide an excellent conformal copper coating that allows the microstructures to be filled with a copper layer having good uniformity using electrochemical deposition techniques. Further, copper layers that are electroplated in the disclosed manner exhibit low sheet resistance and are readily annealed at low temperatures.

The disclosed process, as noted above, is applicable to a wide range of steps used in the manufacture of a metallization layer in a workpiece. The workpiece may, for example, be a semiconductor workpiece that is processed to form integrated circuits or other microelectronic components. Without limitation as to the applicability of the disclosed invention, a process for enhancing a seed layer is described.

A process for applying a metallization interconnect structure to a workpiece

- 9 -

recessed micro-structures, and seed layer enhancement plating are also set forth. A preferred solution for electroplating copper for seed layer enhancement comprises copper sulfate, boric acid, and a complexing agent. The complexing agent is preferably selected from the group consisting of ED, EDTA, and a polycarboxylic acid, such as citric acid. This solution is also suitable for blanket plating and fill-plating of recessed micro-structures.

A plating solution that improves the resistivity of the resulting copper film is also set forth. The plating solution preferably comprises copper sulfate, ammonium sulfate, and ethylene glycol. This solution is also suitable for blanket plating and fill-plating of recessed micro-structures.

- 11 -

Fig. 6A is a scanning eletromicrograph photograph illustrating an ultra-thin seed layer that has been enhanced in a citric acid bath.

Fig. 6B is a scanning eletromicrograph photograph illustrating an ultra-thin seed layer that has been enhanced in an EDTA bath.

Fig. 7 is a schematic representation of a section of a semiconductor manufacturing line suitable for implementing the disclosed seed layer enhancement steps.

- 13 -

of a dielectric 8, such as silicon dioxide. The barrier layer 10 acts to prevent the migration of copper to any semiconductor device formed in the substrate. Any of the various known techniques, such as CVD or PVD, can be used to deposit the barrier layer depending on the particular barrier material being used. Preferably, the thickness for the barrier layer is approximately 100 to 300 Angstroms.

After the deposition of the barrier layer, an ultra-thin copper seed layer 15 is deposited on the barrier layer 10. The resulting structure is illustrated in Fig. 2B. Preferably, the copper seed layer 15 is formed using a vapor deposition technique, such as CVD or PVD. In order to have adequate adhesion and copper coverage, a relatively thick (1000 Angstroms) copper seed layer is usually required. Such a thick seed layer leads to problems with close-off of small geometry trenches, however, when a PVD deposition process is employed for applying the seed layer.

Contrary to traditional thoughts regarding seed layer application, the copper seed layer 15 of the illustrated embodiment is ultra-thin, having a thickness of about 50 to about 500 Angstroms, preferably about 100 to about 250 Angstroms, and most preferably about 200 Angstroms. The ultra-thin copper seed layer can be deposited using a CVD or a PVD process, or a combination of both. PVD is the preferred application process, however, because it can readily deposit copper on the barrier layer 10 with relatively good adhesion. By depositing an ultra-thin seed layer of copper, rather than the relatively thick seed layer used in the prior art, pinching off of

- 15 -

Preferably, the seed layer enhancement process continues until a sidewall step coverage, i.e., the ratio of the seed layer thickness at the bottom sidewall regions 22 to the nominal thickness of the seed layer at the exteriorly disposed side 23 of the workpiece, achieves a value of at least 10%. More preferably, the sidewall step coverage is at least about 20%. Such sidewall step coverage values are present in substantially all of the recessed structures of the semiconductor workpiece. It will be recognized, however, that certain recessed structures distributed within the semiconductor workpiece may not reach these sidewall step coverage values. For example, such structures disposed at the peripheral edges of a semiconductor wafer may not reach these step coverage values. Similarly, defects or contaminants at the situs of certain recessed structures may prevent them from reaching the desired coverage values. The nominal thickness of the enhanced seed layer at the exteriorly disposed side of the workpiece is preferably in the range of 500 angstroms 1600 angstroms.

Although the embodiment of the process disclosed herein is described in connection with copper metallization, it is understood that the basic principle of the enhancement of an ultra-thin seed layer prior to the bulk deposition thereof can be applied to other metals or alloys that are capable of being electroplated. Such metals include iron, nickel, cobalt, zinc, copper-zinc, nickel-iron, cobalt-iron, etc.

A schematic representation of an apparatus 25 suitable for enhancing the

- 17 -

4. pH: 5 – 13, preferably 9.5.

A preferred source of copper ions is copper sulfate (CuSO_4). The concentration of copper sulfate in the bath is preferably within the range of 0.03 to 0.25 M, and is more preferably about 0.1 M.

Complexing agents that are suitable for use in the present invention form a stable complex with copper ions and prevent the precipitation of copper hydroxide. Ethylene diamine tetracetic acid (EDTA), ethylene diamine (ED), citric acid, and their salts have been found to be particularly suitable copper complexing agents. The molar ratio of complexing agent to copper sulfate in the bath is preferably within the range of 1 to 4, and is preferably about 2. Such complexing agents can be used alone, in combination with one another, or in combination with one or more further complexing agents.

The electrolytic bath is preferably maintained at a pH of at least 9.0. Potassium hydroxide, ammonium hydroxide, tetramethylammonium hydroxide, or sodium hydroxide is utilized to adjust and maintain the pH at the desired level of 9.0 or above. A preferred pH for a citric acid or ED bath is about 9.5, while a preferred pH for an EDTA bath is about 12.5. As noted above, the complexing agent assists in preventing the copper from precipitating at the high pH level.

Additional components can be added to the alkaline copper bath. For example, boric acid (H_3BO_3) aids in maintaining the pH at 9.5 when citric acid or ED

- 19 -

from the fact that the magnitude of the voltage potential at which the copper is plated is greater than the magnitude of the voltage potential at which the copper is plated in a bath containing EDTA. This is illustrated in Figs. 4A and 4B where Fig. 4A is a current-potential graph for a citric acid bath, and Fig. 4B is a current-potential graph for an EDTA bath. Electroplating takes place at the voltage where the corresponding current increases abruptly. This plating voltage is referred to as the deposition potential, which is approximately -1.25 volts as shown in Fig. 4A for a bath employing citric acid as the complexing agent, and is approximately -1.0 volts as shown in Fig. 4B for a bath employing EDTA as the complexing agent. The current peaks (70 70' for the a bath containing a citric acid, and 72, 72' for the bath containing the EDTA) are the limiting currents which are mainly determined by mass transfer and the concentration of copper ions in the plating solutions. As illustrated, the magnitude of the current and the particular plating potential is slightly dependent on the substrate material. The different substrate results are illustrated in Figs. 4A and 4B, where 70 and 72 are the curves for a copper substrate material, and 70' and 72' are curves for a copper substrate material comprised of copper with a copper oxide coating. It is noted that additional peaks occur on oxidized copper in the same electrolytes. These peaks are related to the electrochemical reduction of copper oxide to metallic copper before the alkaline electrochemical copper deposition.

- 21 -

sulfate are compared in the graph Fig. 4C. As can be seen, the highest sheet resistance, either with or without annealing at high temperatures, was obtained in the bath containing no ammonium sulfate. If ammonium hydroxide was used to adjust pH in which a trace amount of ammonium sulfate is introduced to the bath, the sheet resistance was reduced from 76 to 23. As the concentration of ammonium sulfate increased from 0.1 M to 0.5 M, the sheet resistance continuously decreased in a corresponding manner.

Although ammonium sulfate assists in reducing the sheet resistance of the deposited copper layer, experimental results indicate that it reduces the conformality of the resulting copper film. However, the addition of ethylene glycol to the ammonium sulfate containing solution substantially increases the conformality of the resulting deposit. Figure 4D illustrates the relationship between the concentration of ethylene glycol and the conductivity of a plating solution containing 0.2M the of ammonium sulfate.

A preferred composition and range of concentrations for the various components of a plating bath having ammonium sulfate include the following:

1. Copper sulfate: 0.03M to 0.5M (preferably, 0.25M);
2. Complexing agent: complex to metal ratios from 1 to 4, preferably 2 using ED;
3. Ammonium sulfate: 0.01M to 0.5M, preferably 0.3M; and
4. Boric acid: 0.00 to 0.5M, preferably 0.2M.

- 23 -

bath comprises 170 g/l H_2SO_4 , 17 g/l copper and 70 ppm Chloride ions with organic additives. The organic additives are not absolutely necessary to the plating reaction. Rather, the organic additives may be used to produce desired film characteristics and provide better filling of the recessed structures on the wafer surface. The organic additives may include levelers, brighteners, wetting agents and ductility enhancers. It is during this deposition process that the trench 5 is substantially filled with a further layer of electrochemically deposited copper 22. The resulting filled cross-section is illustrated in Fig. 2D. After being filled in this manner, the barrier layer and the copper layers disposed above the trench are removed using any suitable process thereby leaving only the trench 5 with the copper metallization and associated barrier material as shown in Fig. 2E.

Use of an alkaline electrolytic bath to enhance the copper seed layer has particular advantages over utilizing acid copper baths without seed layer enhancement. After deposition of the PVD copper seed layer, the copper seed layer is typically exposed to an oxygen-containing environment. Oxygen readily converts metallic copper to copper oxide. If an acid copper bath is used to plate copper onto the seed layer after exposure of the seed layer to an oxygen containing environment, the acid copper bath would dissolve copper oxide that had formed, resulting in voids in the seed layer and poor uniformity of the copper layer deposited on the seed layer. Use of an alkaline copper bath in accordance with the disclosed embodiment avoids

- 25 -

uniformities, as deduced from sheet resistance measurements, of the three wafers after the deposition of a copper layer having a nominal thickness of 1.5 microns.

TABLE 1

<u>Wafer</u>	<u>Enhancement Bath</u>	<u>Current Density</u>	<u>Non-uniformity Standard deviation (%, 1σ)</u>
1	Citrate	3 min. 2mA/cm ²	at 7.321
2	EDTA	3 min. 2mA/cm ²	at 6.233
3	None	0	46.10

As can be seen from the results in Table 1 above, seed layer enhancement in accordance with the disclosed process provides excellent uniformity (6 to 7%) compared to that without seed layer enhancement (46%). This is consistent with observations during visual examination of the wafer after 1.5 micron electroplated copper had been deposited. Such visual examination of the wafer revealed the presence of defects at wafer electrode contact points on the wafer without seed layer enhancement.

Figs. 5, 6A and 6B are photographs taken using a SEM. In Fig. 5, an ultra-thin seed layer has been deposited on the surface of a semiconductor wafer, including micro-structures, such as trenches 85. As shown, void regions are present at the lower corners of the trenches. In Fig. 6A, the seed layer has been enhanced in

- 27 -

individually or in an open carrier through a clean atmosphere joining the tools/tool sets.

In operation, vapor deposition tool/tool set 95 is utilized to apply an ultra-thin copper seed layer over at least portions of semiconductor workpieces that are processed on line 90. Preferably, this is done using a PVD application process. Workpieces with the ultra-thin seed layer are then transferred to tool/tool set 100, either individually or in batches, where they are subject to electrochemical seed layer enhancement at, for example, processing station 110. Processing station 110 may be constructed in the manner set forth in Fig. 3. After enhancement is completed, the workpieces are subject to a full electrochemical deposition process in which copper metallization is applied to the workpiece to a desired interconnect metallization thickness. This latter process may take place at station 110, but preferably occurs at further processing station 115 which deposits the copper metallization in the presence of an acidic plating bath. Before transfer to station 115, the workpiece is preferably rinsed in DI water at station 112. Transfer of the wafers between stations 110, 112, and 115 may be automated by a wafer conveying system 120. The electrochemical deposition tool set 100 may be implemented using, for example, an LT-210TM model or an EquinoxTM model plating tool available from Semitool, Inc., of Kalispell, MT.

Numerous modifications may be made to the foregoing system without

- 29 -

CLAIMS

1. A process for applying a metal structure to a workpiece comprising the step of electroplating a copper layer onto a surface of the workpiece using an electroplating bath comprising copper sulfate, ammonium sulfate, a complexing agent, and ethylene glycol.
2. A process as set forth in claim 1 wherein the electroplating bath further comprises boric acid.
3. A process as set forth in claim 2 wherein the complexing agent is selected from the group consisting of ED, EDTA, and a polycarboxylic acid.
4. A process for applying a metal structure to a workpiece comprising the step of electroplating a copper layer onto a surface of the workpiece using an electroplating bath comprising copper sulfate, boric acid, and a complexing agent.
5. A process as set forth in claim 4 wherein the complexing agent is selected from the group consisting of ED, EDTA, and a polycarboxylic acid.

- 31 -

10. The process of claim 9 wherein the electrochemical deposition step occurs in an alkaline bath.
11. The process of claim 10 wherein the alkaline bath comprises metal ions and an agent effective in complexing the metal ions.
12. The process of claim 7 wherein the ultra-thin metal seed layer formed in step (a) is formed by physical vapor deposition.
13. The process of claim 7 wherein the ultra-thin metal seed layer formed in step (a) has a thickness of about 50 to about 500 Angstroms.
14. The process of claim 13 wherein the ultra-thin metal layer formed in step (a) has a thickness of about 100 to about 250 Angstroms.
15. The process of claim 7 wherein the complexing agent is comprised of one or more complexing agents selected from EDTA, ED, and polycarboxylic acid.
16. The process of claim 11 wherein the complexing agent is comprised of EDTA and the EDTA in the bath has a concentration within the range of 0.03 to 1.0 M.

- 33 -

22. In a manufacturing line including a plurality of apparatus for the manufacture of integrated circuits, one or more apparatus of the plurality of apparatus being used for applying a copper metallization interconnect structure to a surface of a workpiece used to form the integrated circuits, the one or more apparatus comprising:

means for applying a conductive ultra-thin seed layer to a surface of the workpiece;

means for electrochemically enhancing the conductive ultra-thin seed layer to render it suitable for subsequent electrochemical application of the copper interconnect metallization to a predetermined thickness representing a bulk portion of the copper interconnect metallization structure.

23. One or more apparatus as claimed in claim 22 wherein the means for applying is further defined by means for applying a conductive ultra-thin copper seed layer to a barrier layer surface of the workpiece.

24. One or more apparatus as claimed in claim 22 wherein the means for applying is further defined by means for applying a conductive ultra-thin copper seed layer to a barrier layer surface of the workpiece using a PVD process.

- 35 -

30. One or more apparatus as claimed in claim 26 wherein the complexing agent is comprised of ED.
31. One or more apparatus as claimed in claim 26 wherein the complexing agent is a comprised of a carboxylic acid or salt thereof.
32. One or more apparatus as claimed in claim 31 wherein the complexing agent is citric acid or salt thereof.
33. One or more apparatus as claimed in claim 26 and further comprising means for electrochemically adding a further layer of copper over the conductive ultra-thin seed layer by electrochemically depositing copper using an acidic copper bath.
34. One or more apparatus as claimed in claim 33 wherein the electrochemical enhancement of the ultra-thin seed layer takes place at a plating voltage having a magnitude that is greater than the magnitude of the plating voltage in the acidic copper bath.

- 37 -

39. The process of claim 38 wherein the ultra-thin seed layer formed in step (a) has a thickness of about 100 to about 250 Angstroms.
40. The process of claim 39 wherein the ultra-thin seed layer formed in step (a) has a thickness of about 200 Angstroms.
41. The process of claim 36 wherein the alkaline electrolytic bath has a pH of at least 9.0.
42. The process of claim 36 wherein the copper ions in the electrolytic bath are provided by copper sulfate.
43. The process of claim 42 wherein the copper sulfate in the electrolytic bath has a concentration within the range of 0.03 to 0.25 M.
44. The process of claim 42 wherein the concentration of copper sulfate is about 0.1 M.
45. The process of claim 36 wherein the copper complexing agent is comprised of a copper complexing agent selected from EDTA, ED, and citric acid.

- 39 -

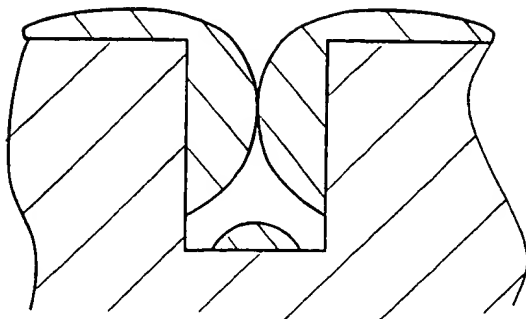
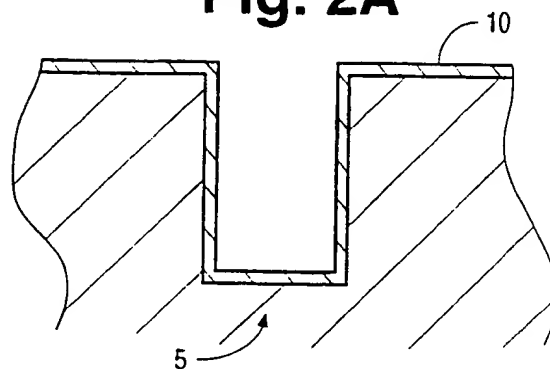
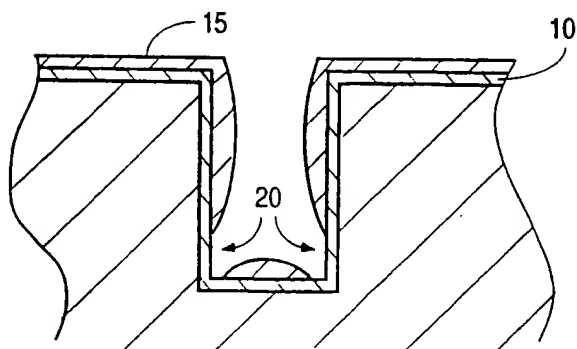
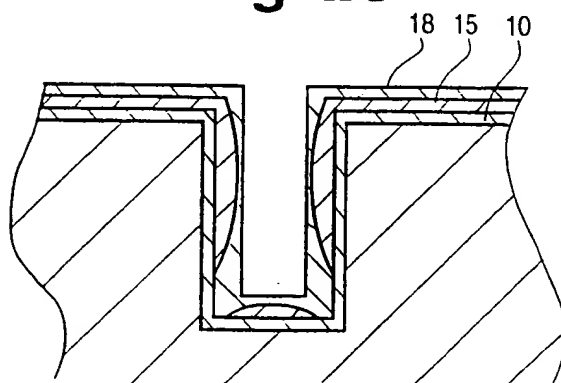
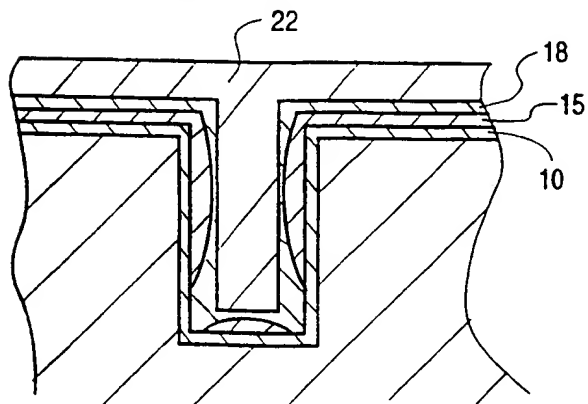
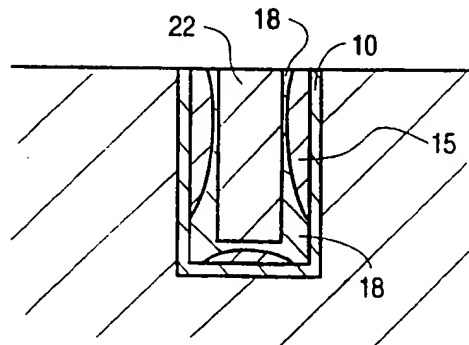
electrolytic solution to complete deposition of the copper to a thickness needed for the formation of the copper interconnect structure.

52. The process of claim 51 and further comprising the step of subjecting the workpiece to a rinsing process after step (b) and prior to the further electrochemical copper deposition process in an acidic electrolytic solution.

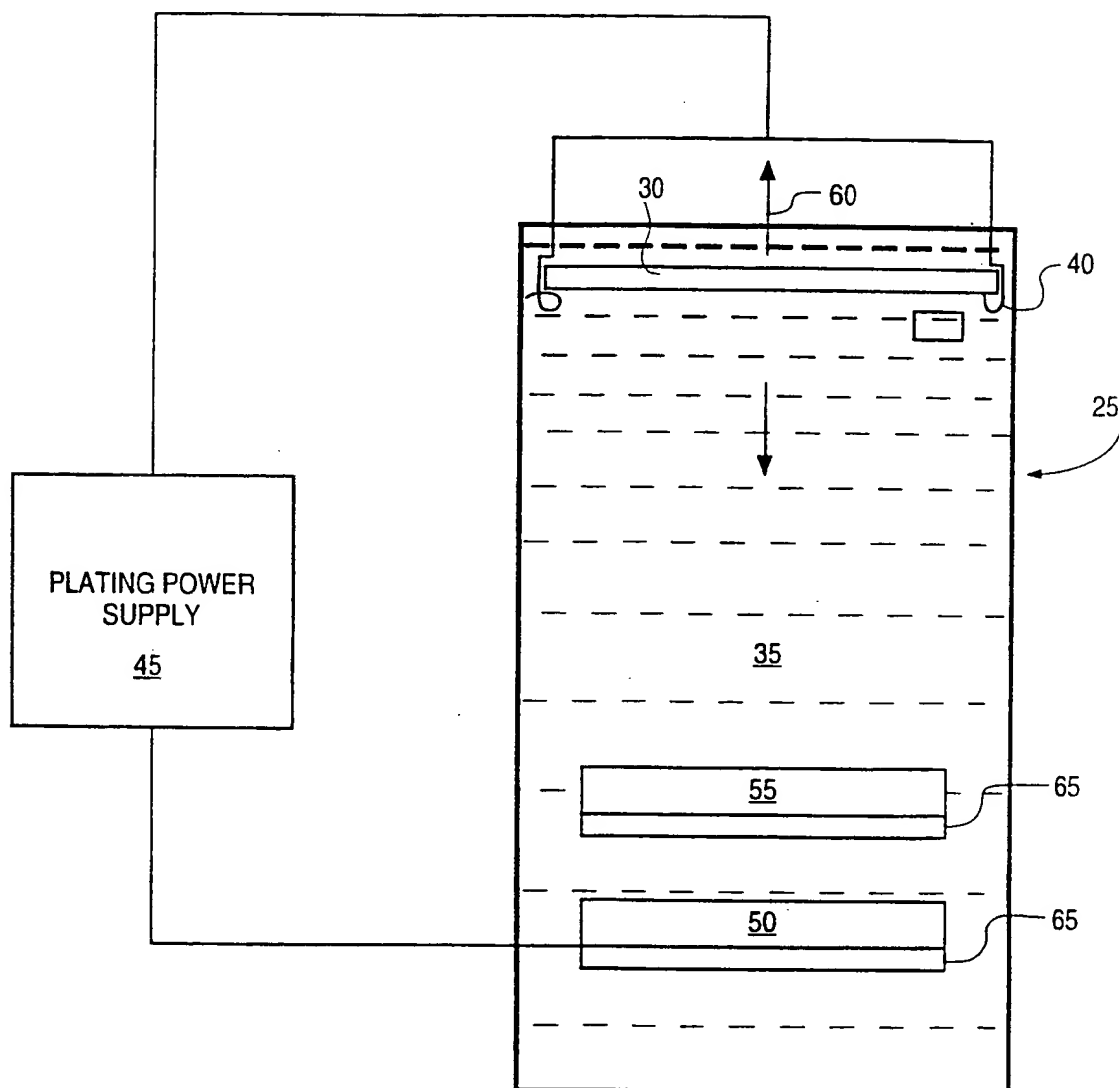
53. A workpiece comprising:
a plurality of the recessed structures distributed in a face of the workpiece;
an enhanced seed layer having a thickness at all points on sidewalls of substantially all recessed features distributed within the workpiece that is equal to or greater than about 10% of the nominal seed layer thickness over an exteriorly disposed surface of the workpiece.

54. A workpiece as claimed in claim 54 wherein the thickness of the sidewalls of substantially all recessed features is equal to or greater than about 20%.

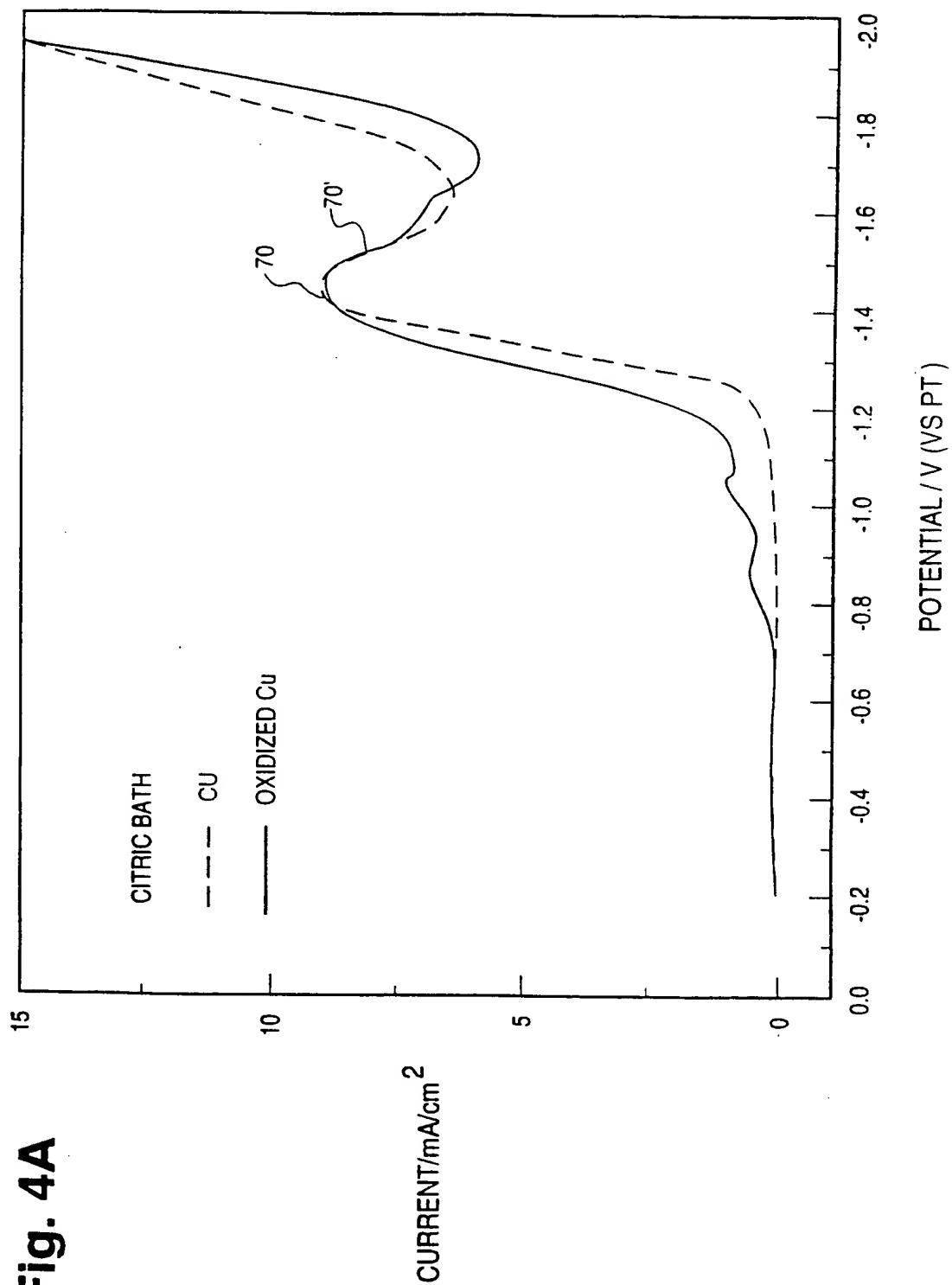
55. A solution for electroplating copper, the solution comprising copper sulfate, ammonium sulfate, and ethylene glycol.

Fig. 1**Fig. 2A****Fig. 2B****Fig. 2C****Fig. 2D****Fig. 2E**

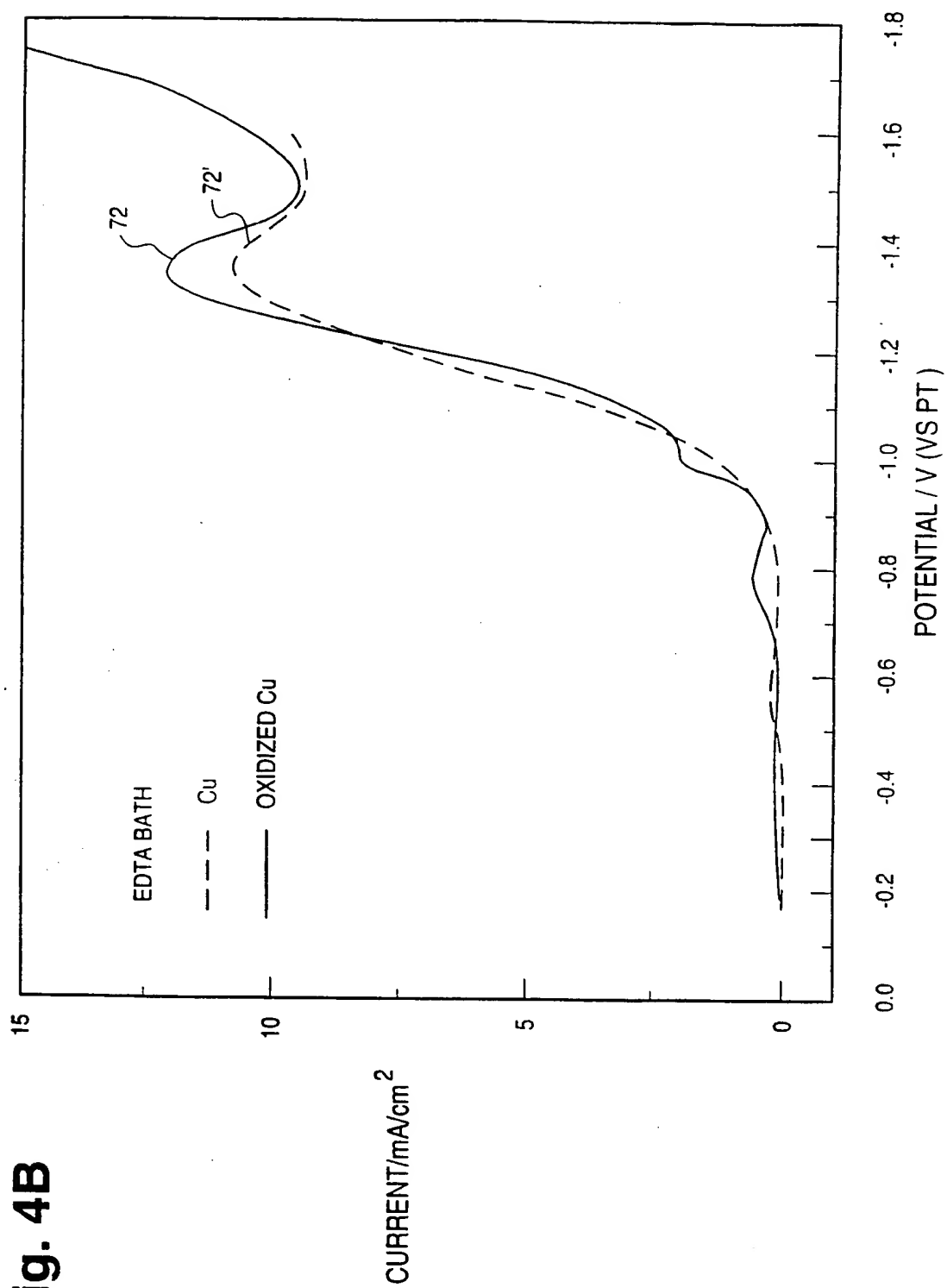
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Fig. 3

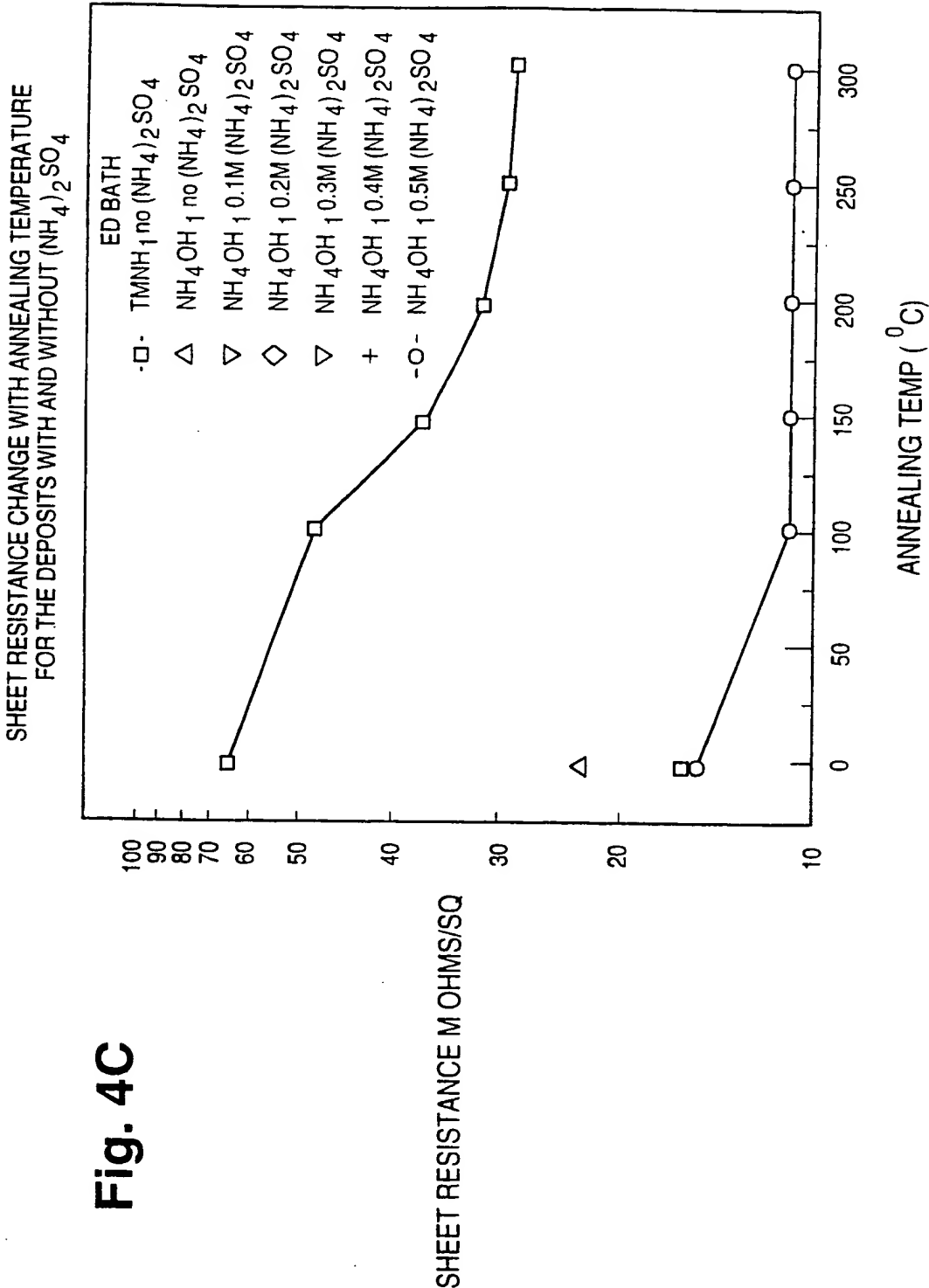
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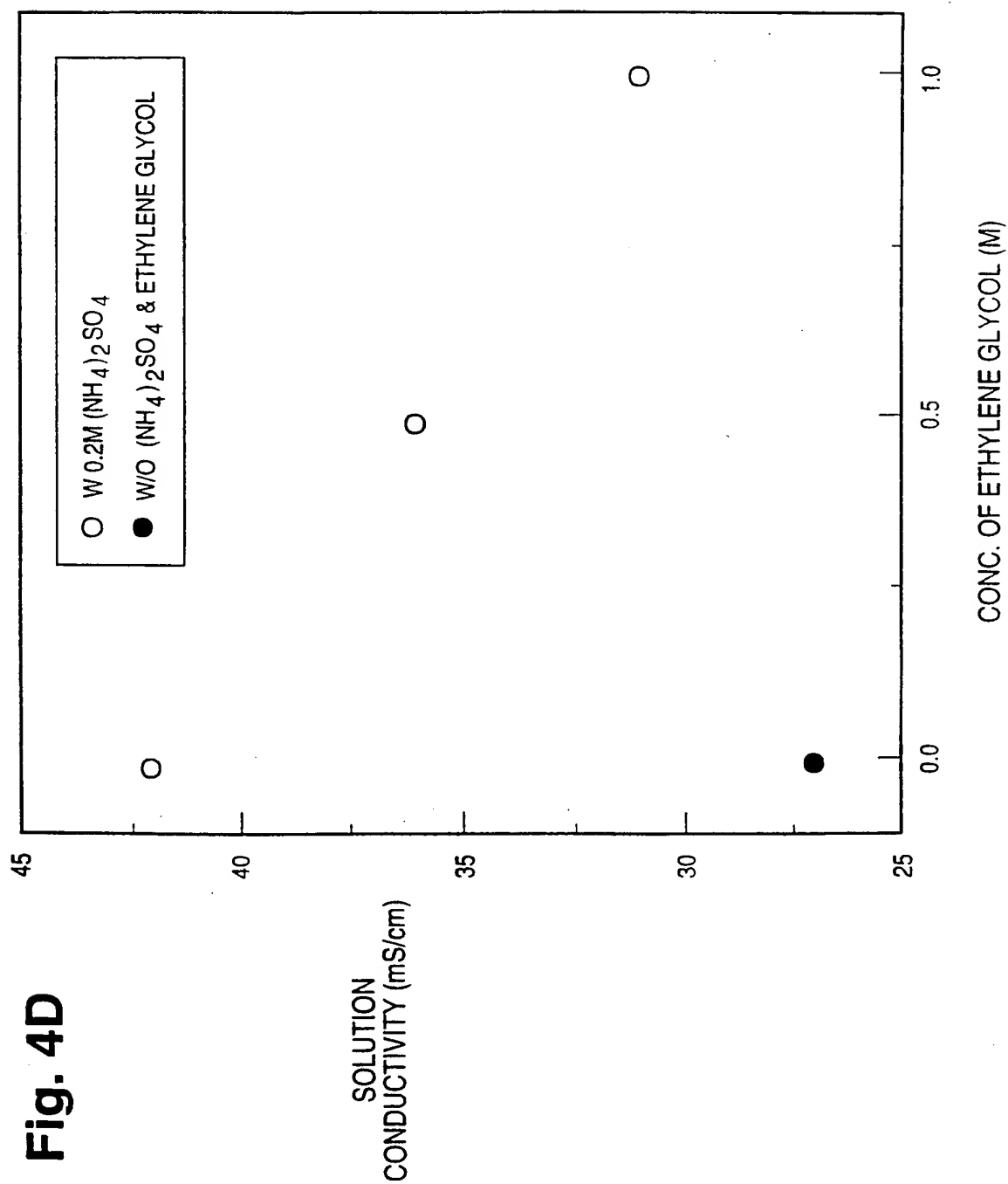
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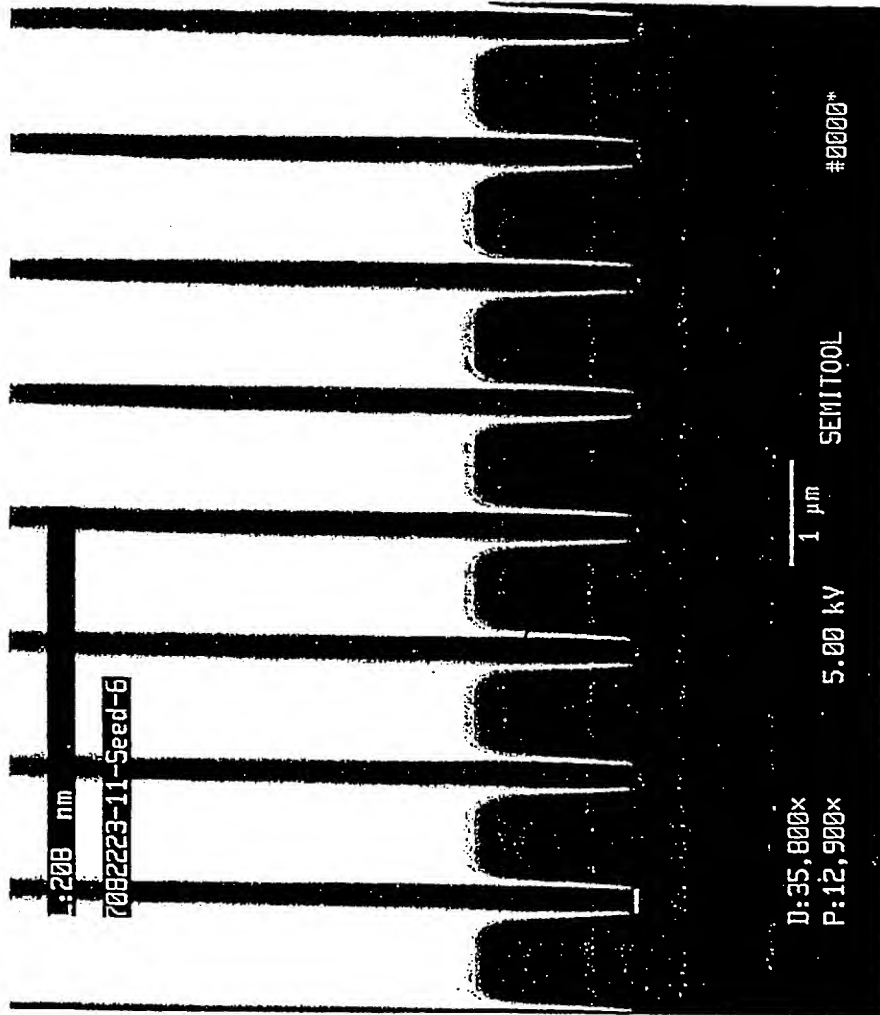
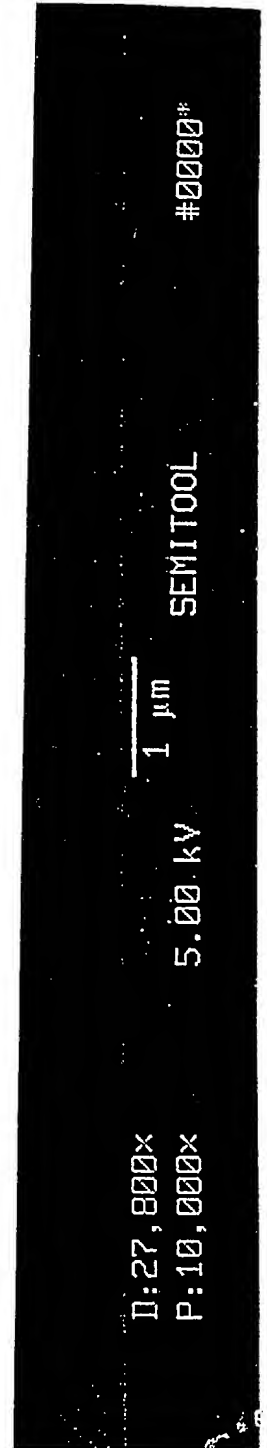


Fig. 5

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Fig. 7